REMARKS

The Office Action dated May 25, 2005 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 9-16 have been allowed. Claims 1-8 are submitted for consideration.

As a preliminary matter, Applicant wishes to thank the Examiner for allowing claims 9-16.

Claims 2-5 were objected to as being dependent on a rejected base claim. The Office Action indicated that claims 2-5 contain allowable subject matter, and would be allowable if amended to be in independent form. Based on the arguments present below, Applicant submits that claim 1, upon which claims 2-5 depend, is allowable and thus the objection of claims 2-5 should be withdrawn.

Claims 1, 6, 7 and 8 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,268,656 to Muscavage. The rejection is traversed as being based on a reference that neither teaches nor suggests the novel combination of features clearly recited in any of claim 1, 6, 7 and 8.

Claim 1, upon which claims 2-7 depends, recites a method including generating a first clock signal and generating a plurality of clock signals, each having different phases. The method also includes generating a second clock signal based on the plurality of clock signals, the second clock signal having a different phase from the first clock signal and outputting the first and second clock signals.

Claim 8 recites a system including means for generating a first clock signal and means for generating a plurality of clock signals, each having different phases. The system also includes means for generating a second clock signal based on the plurality of clock signals, the second clock signal having a different phase from the first clock signal and means for outputting the first and second clock signals.

As outlined below, Applicant submits that the cited reference of Muscavage does not teach or suggest the elements of claims 1, 6, 7 and 8.

Muscavage teaches a clock generation circuit which includes an oscillator and which receives a reference clock signal and generates an oscillator clock signal as output. The output of the oscillator clock signal is a multiple of the frequency of a desired or programmed clock signal selected by a user. The desired clock signal is generated to clock devices on a circuit board on which the integrated circuit containing the clock skew adjustment circuit is mounted. Col. 2, lines 31-64 and Figure 1. The oscillator is a multiple stage oscillator in which stages are substantially identical. Outputs are tapped off selected ones of the stages of the oscillator to provide a plurality of phases of the oscillator clock signal. The number of oscillator clock phases generated is dependent on the configuration of the oscillator and the number and increment size of desired or programmed clock phases to be generated. Each oscillator stage output provides clock phase as a clock signal to each of a plurality of ring counters or shift registers. Each stage of the multiple stage ring shift register is preset upon powering up and is designated by a number. Each stage provides an output to a multiplexer and the next succeeding

stage of the multiple stage ring shift register. The multiplexer is controlled to select one of the inputs as an output. Col. 2 line 65 – Col. 3, line 65 and Figures 2 and 5.

Applicant submits that Muscavage fails to teach or suggest each of the elements of claims 1, 6, 7 and 8. Claims 1 and 8 recite generating a first clock signal, generating a plurality of clock signals, each having different phases, generating a second clock signal based on the plurality of clock signals, the second clock signal having a different phase from the first clock signal and outputting the first and second clock signals. The Office Action states that Muscavage teaches that the oscillator generates a first clock as recited by claims 1, 6, 7 and 8. However, there is simply no showing or suggestion in Muscavage of the oscillator generating the first clock signal as recited in claims 1, 6, 7 and 8. Muscavage shows in figure 2 that the oscillator generates a plurality of clock signals, where each clock signal generated by an oscillator stage is outputted to the shift registers. Thereafter, according to Muscavage, the multiplexer selects one of the outputs from the shift registers as an output, which the Office Action states is the second clock signal as recited in claims 1, 6, 7 and 8. If as the Office Action suggests the output of the multiplexer, in Muscavage, is the second clock signal, recited in claims 1, 6, 7 and 8, then there is simply no teaching of suggestion in Muscavage of outputting the first and second clock signals as recited in claims 1, 6, 7 and 8. Figures 2 and 5 of Muscavage only show that there is one output, i.e., the output of the multiplexer. As such, there is no teaching or suggestion in Muscavage of outputting the first and second clock signals. Furthermore, since Muscavage does not teach or suggest the first clock signal, it also

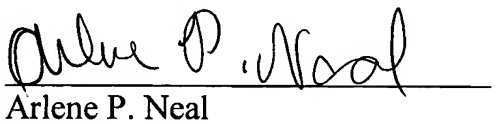
does not teach or suggest that the second clock signal has a different phase from the first clock signal as recited in claims 1, 6, 7 and 8. Therefore, Applicant respectfully asserts that the rejection under 35 U.S.C. §102(b) should be withdrawn because Muscavage simply does not teach or suggest each feature of claims 1 and 8 and hence, dependent claims 2-7 thereon.

As noted previously, claims 1-8 recite subject matter which is neither disclosed nor suggested in the prior art reference cited in the Office Action. It is therefore respectfully requested that all of claims 1-16 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Arlene P. Neal
Registration No. 43,828

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

APN:mm